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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,386	04/23/2001	Yoshihisa Matsubara	NEKA 18.612	2510

26304 7590 01/21/2004

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EXAMINER	
VINH, LAN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 01/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/840,386	MATSUBARA ET AL.	
	Examiner	Art Unit	
	Lan Vinh	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-11* is/are pending in the application.

4a) Of the above claim(s) *4-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/840386* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohashi et al (US 6,376,345) in view of Matsuo et al (US 6,296,714)

Ohashi discloses a process for manufacturing semiconductor device comprises the steps of :

forming N-type region and P-type region on a substrate 1 (col 11, lines 20-22), forming wiring 28, 26 to connect the N and P-type region (col 11, lines 36-37; fig. 7)

performing a cleaning step of the semiconductor wafer in portion 160 using a weak alkaline chemical solution (col 12, lines 15-17, col 14, lines 5-8, fig. 7 shows that the upper surface of wiring 28 is exposed during the cleaning step), which reads on performing a processing step on a semiconductor substrate on which the upper surface of the wiring is exposed using a liquid

illuminating the semiconductor wafer/substrate during the cleaning/process step (col 15, lines 1-3; col 17, lines 26-29), which reads on radiating light on the semiconductor substrate when performing the cleaning/process step

Ohashi also discloses that the cleaning/processing step is performed after a CMP (chemical mechanical polishing) step (col 16, lines 5-18)

Unlike the instant claimed invention as per claim 1, Ohashi does not specifically disclose illuminating/radiating light having wavelength of 500 nm to less than 1microns on the semiconductor substrate

However, Matsuo discloses a method of washing semiconductor substrate comprises the step of radiating light having wavelength of 500 nm to 900 nm (overlaps the claimed range of 500nm to less than 1 microns) on the semiconductor substrate during washing/cleaning (col 6, lines 51-53)

Since both Ohashi and Matsuo are concerned with the step of illuminating the semiconductor substrate during cleaning, one skilled in the art would have found it obvious to modify Ohashi's method by radiating light having wavelength of 500 nm to 900 nm on the semiconductor substrate during washing/cleaning as per Matsuo because according to Matsuo when light is irradiated at the washing, a wavelength of light to be irradiated to the semiconductor substrate is preferably 500-900 nm thus an effect of removing metal impurities near the surface of the substrate is heightened (col 6, lines 54-63)

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohashi et al (US 6,376,345) in view of Matsuo et al (US 6,296,714) and further in view of Klebanoff (US 6,169, 652)

Ohashi as modified by Matsuo has been described above. Unlike the instant claimed invention as per claim 2, Ohashi and Matsuo do not disclose that the

processing/cleaning step is performed in a state in which the semiconductor substrate is grounded.

However, Klebanoff, in a method of using different chucks to hold semiconductor wafer during processing, teaches maintaining/controlling the semiconductor substrate at zero voltage (ground potential) during processing (col 3, lines 15-17)

Since both Ohashi and Matsuo are concerned with the step of cleaning the semiconductor substrate, one skilled in the art would have found it obvious to modify Ohashi and Matsuo method by maintaining/controlling the semiconductor substrate at zero voltage (ground potential) during processing as per Klebanoff because Klebanoff states that employing a voltage-controlled electrostatic chuck will significantly reduce the likelihood of contaminant deposition on the substrate (see abstract).

Response to Arguments

4. Applicant's arguments filed 11/10/2003 have been fully considered but they are not persuasive.

Applicants argue that the Ohashi reference does not show or suggest a light source radiating light onto the semiconductor substrate because Ohashi teaches shading the first major surface of the wafer such that an illuminance of the first major surface of the wafer is 500 lux or less. This argument is unpersuasive because although the examiner recognizes that Ohashi teaches shading the first major surface of the wafer such that an illuminate of the first major surface of the wafer is 500 lux or less, Ohasi teaching of "an illuminance of the first major surface of the wafer is 500 lux" does not exclude the use of

radiating light on the semiconductor substrate. Thus, the examiner asserts that Ohasi reference suggests radiating light onto the semiconductor substrate.

It is also argued that neither Ohashi nor Matsuo suggest a cleaning step performed during or before a CMP process because Ohashi discloses performing the cleaning step after a CMP. The examiner disagrees because claim 1 requires that "a cleaning step performed during, before or after a step that include CMP" and Ohashi discloses performing the cleaning step after a CMP, the examiner asserts that Ohashi disclosure reads on claim 1.

In response to applicant's argument that there is no suggestion to combine the references of Ohashi and Matsuo/the combination of Ohashi with Matsuo would not lead a skilled artisan to the present invention, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, since Ohashi suggests radiating light on the substrate in a cleaning step and Matsuo teaches the advantage of radiating light having wavelength of 500 nm to 900 nm on the semiconductor substrate during cleaning (paragraph 2), one skilled in the art would have found it obvious to incorporate Matsuo teaching into Ohashi method to produce the claimed invention.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 571 272 1471. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571 272 1465. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

LV
January 9, 2004